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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,996	08/04/2003	Dirk Fuhrmann	P2002,0648	5011

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EXAMINER	
ELLIS, KEVIN L	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,996	FUHRMANN ET AL.	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,14 and 16* is/are rejected.

7)☒ Claim(s) *5-13, 15, and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 are presented for examination.

2. Information disclosed and listed on PTO 1449 has been considered.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-3, 14, and 16 are rejected under 35 U.S.C. § 102(e) as being anticipated by Phan, U.S. Patent 6,651,202.

A) As to claim 1, Phan discloses the invention as claimed. There is a memory (Fig 1) that has memory cells for storing data, the memory is capable of being accessed for reading and writing to the memory cells. The memory also has integrated with it address calculation logic for generating addresses to test the memory cells (see Fig 1 and Col 5 Lines 17-27, 42-53, and Col 6 Lines 19-60).

B) As to claim 2, the memory of Phan does receive address, command, and data signals (see Fig 1).

C) As to claim 3, the address calculation logic does operate with a clock signal (see Fig 1).

D) As to claim 14, the memory is addressed with column and row addresses which would be calculated by the address calculation logic unit (see Col 5 Lines 41-46).

E) As to claim 16, the BIST of Phan is initialized with parameters for testing the memory, the address calculation logic activated, and the signals necessary are applied to the memory cells being tested (see Fig 3A).

Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 14, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fleischman et al., U.S. Patent 6,321,320.

A) As to claim 1, Fleischman et al. discloses the invention substantially as claimed. There is a memory (Fig 2 & 3) that has memory cells for storing data, the memory is capable of being accessed for reading and writing to the memory cells. The memory also has integrated with it address calculation logic for generating addresses to test the memory cells (see Fig 3 and Col 5 Lines 21-44). However, the memory of Fleischman et al. is part of a processor chip and not a stand alone memory. The advantages of the BIST

taught by Fleischman et al. (see Col 3 Lines 25-36) would also apply to a stand alone memory and not just a memory that is part of a processor chip. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the BIST of Fleischman et al. would be utilized in a stand alone integrated memory and provide the same advantages as taught by Fleischman et al.

B) As to claim 2, the address calculation logic does received signals for the test operation (see Col 5 Lines 21-44).

C) As to claim 3, the address calculation logic does operate with a clock signal (see Col 18 Lines 4-16).

D) As to claim 4, there are registers for storing information for the address calculation logic (see Fig 4 and Col 7 Lines 1-39).

E) As to claim 14, the memory array of Fleischman et al. would have rows and columns as other memory arrays do. This would mean that the address calculation logic would also calculate the row and column address for the memory cell being tested.

F) As to claim 16, the BIST of Fleischman et al. is initialized with parameters for testing the memory, the address calculation logic activated, and the signals necessary are applied to the memory cells being tested (see Col 5 Lines 20-44, Col 7 Lines 1-39).

Allowable Claims

7. Claims 5-13, 15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
September 14, 2005